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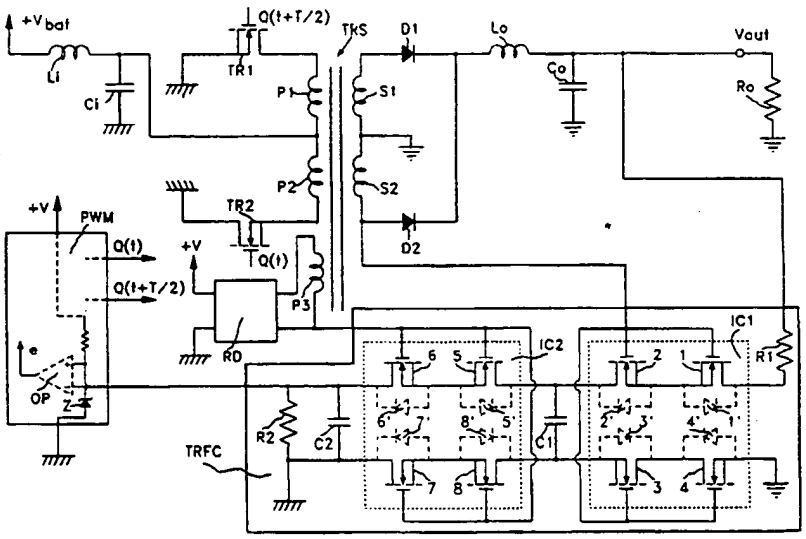

(57) Abstract

DC/DC converter using a transformer to galvanically insulate the load from the primary power supply source, to ensure said insulation even along the feedback path, thanks to a charge-transfer network inserted along said path. Said network consists essentially of two capacitors (C1) and (C2) and two pairs of synchronous electronic switches (IC1) and (IC2) provided with MOSFETs. The pair IC1 when closed connects C1 in parallel with the load R_o, while IC2 when closed connects C1 in parallel with C2, which has one end connected to the primary ground. The pairs IC1 and IC2 are controlled by two respective periodic signals, which are mutually decoupled through the transformer and correspond to the signals used for switching the two power transistors of the converter in push-pull configuration.

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"DC/DC converter comprising a high-insulation charge-transfer feedback network"

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DESCRIPTION

The present invention relates to the field of DC/DC converters and specifically to a DC/DC converter comprising a high-insulation charge-transfer feedback network.

The operating principles of DC/DC converters just as the numerous circuit configurations based on these principles have been long known. An exhaustive treatment of this subject matter is given e.g. in the volume of LLoyd Dixon Jr entitled "Switching Power Supply Topology Review", published by the UNITRODE CORPORATION following the Power Supply Design Seminar held in Lexington (USA) in 1985.

Design of a DC/DC converter is greatly facilitated today by the fact that special integrated circuits capable of performing all the main control functions of the converter are commonly available. Said circuits comprise essentially, (a) a presettable frequency oscillator from which are taken the waveforms useful for controlling electronic switches, (b) a constant temperature-stabilized reference voltage generator, c) an operational amplifier calculating the difference between the constant reference voltage and the voltage on the load obtaining an error signal, and d) a feedback network which, on the basis of the error signal, produces a modulation of the duration of the oscillator pulses to stabilize the voltage on the load.

Often, for reasons of safety both of persons and of the equipment powered by the DC/DC converter, there is also required a galvanic insulation between the primary power supply source of the converter and the load. For this purpose a transformer is nearly always used. However the transformer alone is insufficient to ensure galvanic insulation since, through the feedback network, there could be generated a direct connection path between the primary-side circuits and the secondary-side circuits. It is accordingly necessary to take appropriate measures in the feedback network in order to preserve the above mentioned insulation.

A first known solution uses an auxiliary primary winding on the transformer connected to a bridge, and to a low-pass filter. At the output of the filter is a d.c. voltage whose level varies in proportion to the secondary voltage, and it can therefore be used for generation of the error signal. The main shortcoming of this first solution is that if there is a variation in the direct junction voltage of the diodes which rectify the secondary current, or in the voltage at the terminals of any components in series with the load, the voltage on the load also

varies without the feedback network detecting the variation, because the feedback network is sensitive only to the sum of these voltages.

A second known solution uses an optical coupler to transfer the voltage error to the rest of the feedback network. The main shortcoming of this second solution is the fact that the optical coupler introduces a low-frequency pole in the closed-loop response, linked to the low operating speed of these components typically below 10kHz. Owing to the known stability criteria, it is advisable to have a converter loop-gain frequency response behaviour similar to that of a single-pole function. It is therefore necessary to neutralize the pole introduced by the optical coupler by means of the introduction in the feedback loop of a dominant-zero network, but this is difficult to implement for the following reasons: (a) the broad variability of the physical parameters found in optical coupler production batches, and (b) the strong dependence on temperature of the optical coupler pole frequency.

A practical way to compensate for the variability of type (a) above, is to generate an error signal upstream of the optical coupler to force the feedback loop to activate the above mentioned compensation automatically. By so doing however, it is no longer possible to use the differential comparator and reference voltage generator in the integrated circuit controlling the converter, and it thus becomes necessary to use further electronic components. Contrary to what takes place for (a) above, it is difficult to compensate for the thermal effects mentioned under (b) above, and in any case the compensation introduced is only partial and not repetitive.

The basic problem solved by the optical coupler and which must be solved by any device or circuit replacing it, is to transfer a slowly varying voltage, like the error voltage, between two mutually decoupled points.

A circuit which in a first analysis could solve this problem is described in international patent application PCT WO-A-86/01653. In reality this document describes and claims two different circuits of which the first is denominated "Capacitive voltage transformer" (see FIG. 4 annexed), and a second, closer to a charge-transfer network used in the present invention, is a "decoupling stage" used to separate the load equipment from the mains lines or from a d.c. voltage (see FIG. 2). This separation is implemented by a switching circuit comprising two double electronic switches working in phase opposition between the input and output points. These switches are controlled by a square-wave frequency generator which can be achieved by squaring the wave form of the alternating voltage on the main lines. In the description it is also stated that the alternating voltage has a period of 50 or 60 cycles and that for control of the electronic

switches an optical coupler can be used optionally.

The teaching of the PCT patent could lead a person skilled in the art intending to remove the shortcomings caused by the optical coupler in the feedback network of a DC/DC converter, to duly consider the possibility of replacing the optical coupler with the decoupling stage, as stated in the description. But this would involve two serious shortcomings which would make a mere replacement unfeasible. A first shortcoming would be the lack of galvanic insulation and a second that of the insufficiency of the error signal which would be generated. The first shortcoming could be remedied as suggested in the text, i.e. by using at least one optical coupler for control of the electronic switches. But this would again introduce the above mentioned shortcomings it was sought to remove, and essentially attributable to the neutralization of a low-frequency pole and its temperature compensation. In this case the pole in the loop gain would be caused by the fact that a variation in the load voltage faster than the switching time of the optical coupler would be only partially felt or not felt at all.

As regards the reintroduction of the optical coupler, it should not be considered a possibility, but an essential requisite for achieving insulation between the two points to be decoupled. Indeed, to provide the square-wave generator G_f (indicated only schematically in FIG. 2) it is necessary to have a squaring circuit followed by an inverter inevitably connected to the main lines, after which the two double switches would be respectively controlled by the true or inverted wave form. Lacking an optical coupler, it is necessary to have a common reference point for the voltages on the control electrodes of the transistors constituting the two double electronic switches, thus losing the galvanic insulation between them. By using instead an optical coupler for control of the double switch connected to the load and powering the optical coupler transistor with the voltage on the load, it would no longer be necessary to connect together the two grounds and the galvanic insulation would be preserved.

As regards the second shortcoming, i.e. insufficiency of the error signal, it is immediately apparent that the decoupling stage described in the PCT patent transfers a voltage in an essentially discontinuous manner. Indeed, when one double switch is closed towards the main lines, the other is open and the load is not powered for the duration of a half-wave. This type of operation is not limiting in slow applications, such as for example in the case of igniting a lamp, but can be unacceptable if the duration of the closing of the switches can be very short in relation to their open time, as takes place in the context of the present invention. In these cases, as will also be seen below, the ability to transfer a portion of the charge accumulated in the first capacitor to a second capacitor, which supplies the

voltage at the point where it is needed when the first capacitor is disconnected, becomes basic. It is just the presence of a second capacitor which can qualify the decoupling stage mentioned above as a charge-transfer network.

Lastly there is analyzed another cause which could contribute to loss of galvanic insulation, again with reference to the above mentioned decoupling stage. This depends on the fact that there is used a square wave to control the electronic switches, which involves simultaneous switching of the two double switches, upon the arrival of the edge wave. As known, to move from conduction to interdiction the active devices, making up the above mentioned switches, employ a given time period during which a direct path remains between the two points to be decoupled.

Accordingly the purpose of the present invention is to overcome all the above shortcomings and indicate a DC/DC converter comprising a high-insulation charge-transfer feedback network.

To achieve these purposes the object of the present invention is a DC/DC converter using a transformer to galvanically insulate the load from the primary power supply source, while ensuring said insulation along the feedback path also, thanks to a charge-transfer network inserted along said path. The network consists essentially of two capacitors and two pairs of electronic switches provided by means of solid-state devices. A first pair of switches, when closed, connects a first capacitor in parallel to the load. The second pair connects the first capacitor in parallel to the second which has one end connected to the primary ground. The two pairs of electronic switches are controlled by two respective periodic signals decoupled from each other through the transformer and corresponding to the signals used for the switching of two power transistors of the converter in a push-pull configuration. During each period of the control signals there succeed four phases in which: in a first phase the first capacitor is charged at the value of the voltage at the ends of the load; in a second phase the two pairs of switches are both open; in a third phase the charge of the first capacitor is partly transferred to the second; and in a fourth phase the two pairs of switches are still both open. At the ends of the second capacitor there is thus created a fraction of the load voltage even though the capacitor is insulated galvanically from the load as it is explained in claim 1.

The DC/DC converter which is the subject matter of the present invention exhibits the basic advantage of always ensuring perfect galvanic insulation between the load and the primary source. When off, insulation is achieved thanks to the use of enhancement MOSFETs in the charge-transfer network. During operation, insulation is achieved thanks to the particular circuit structure of the charge-transfer network and to the use of control signals decoupled from each

other by means of the transformer. The use of optical couplers is thus entirely superfluous for control of the electronic switches. Furthermore, as the control signals are mutually phase by shifted one half period and have a duty cycle below 0.5, all possibility of simultaneous closing of the two switch pairs is eliminated due to the finite time taken by the active devices to change over from conduction to interdiction. Specifically, closing of a generic switch pair is always preceded and followed by phases in which both switch pairs are open.

A second advantage of the converter which is the subject matter of the present invention lies in its intrinsic stability due to the fact that the charge control network works at a frequency of about 120kHz, without introducing appreciable phase delay in the loop band, which is typically 12kHz wide. There is therefore no low-frequency pole to be neutralized and compensated thermally. It is also possible, given the invariance of the physical parameters of the charge-transfer network, to use the reference voltage and the differential comparator in the integrated circuit which controls the converter.

A third advantage is due to the fact that each switch is provided by means of two MOSFETs having their source connected to the respective substrates. The same channel current flows in the transistors, one in direct- and the other reverse-conduction. Consequently the diodes formed between the drain-substrate junctions are back-to-back connected. This ensures insulation even through the substrate.

Further purposes and advantages of the present invention are clarified in the detailed description of an embodiment thereof given below by way of nonlimiting example with reference to the annexed drawings wherein:

The only figure (FIG. 1) shows an indicative circuit diagram of the DC/DC converter which is the subject matter of the present invention wherein the charge-transfer network TRFC included in the feedback path is clearly shown.

The DC/DC converter of FIG. 1 comprises two power transistors TR1 and TR2 respectively connected between the two ends of the primary winding of a transformer TRS and a primary ground common to the negative terminal of a battery (not shown in the FIG.) supplying a continuous voltage +Vbat. The positive terminal of the battery is connected to one end of an inductor Li whose other end is connected to a central tap of the TRS primary. The latter divides the primary in two half-windings P1 and P2. The central tap of the primary is also connected to one end of a capacitor Ci which has its other end connected to the primary ground. The secondary of the transformer is also divided in two half-windings S1 and S2 by a central tap connected to a secondary ground galvanically insulated from the primary ground. The two ends of S1 and S2 are respectively connected to the

anodes of two diodes D1 and D2 whose cathodes are both connected to one end of and inductor Lo which has the other end connected to the output terminal of the DC/DC converter. A capacitor Co is connected between the output terminal and the secondary ground, and in parallel with Co is visible a load resistance Ro at whose ends the continuous output voltage Vout is present.

The transformer TRS has another primary winding P3 which supplies a rectifier circuit RD, which supplies a d.c. voltage +V to an integrated circuit PWM which generates two signals indicated by Q(t) and Q(t+T/2) respectively, and applied to the control electrodes of the transistors TR1 and TR2. The voltage +V is also used by converter protection circuits connected like PWM to the primary ground and not shown in the figure for the sake of simplicity.

In the integrated circuit PWM is present an operational amplifier OP whose non-inverting input is connected to the cathode of a Zener diode Z (which diagrams a reference voltage generator), and whose inverting input is connected to the output of a charge-transfer network TRFC optionally through a potentiometric voltage divider not shown in the figure. The anode of the Zener diode Z is connected internally to the primary ground and the cathode is connected to the power supply +V by means of circuits diagrammed with a resistance. At the output of the operational amplifier OP is present an error signal e used in the integrated circuit PWM to generate the signals Q(t) and Q(t+T/2).

The charge-transfer network TRFC consists of two integrated circuits IC1 and IC2, two capacitors C1 and C2 and two resistors R1 and R2. Each integrated circuit IC1 and IC2 comprises four identical n-channel enhancement MOSFET transistors respectively indicated by 1, 2, 3, 4 and 5, 6, 7, 8. Use of the p-channel MOSFETs instead of n-channel MOSFETs does not change operation of the network. All the transistors have their substrate (type p) connected to the respective source. In IC1 and IC2 are also visible diodes (1', ... 8') corresponding to those existing between the drain and the substrate of respective transistors. The gates of the MOSFETs 1, 2, 3 and 4 are all connected together and to one end of the secondary S2 connected to the diode D2. The gates of the MOSFETs 5, 6, 7 and 8 are all connected together and to one end of the primary winding P3. In the integrated circuit IC1 the MOSFETs 1 and 2 have their sources connected together and the MOSFETs 3 and 4 have their drains connected together. In the integrated circuit IC2 the MOSFETs 5 and 6 have their sources connected together as do the MOSFETs 7 and 8.

The resistance R1 is connected between the output terminal of the converter and the drain of the MOSFET 1. The capacitor C1 has one end connected to the drains of the MOSFETs 2 and 5 and the other end connected to

the drain electrode of the MOSFET 8 and the source of the MOSFET 3. The source of the MOSFET 4 is connected to the secondary ground. The capacitor C2 has one end connected to the drain of the MOSFET 6 while the other end of C2 is connected to the drain of the MOSFET 7 and to the primary ground. The resistance R2 is connected in parallel with C2 and with the inverting input of the operational amplifier OP in the integrated circuit PWM.

As concerns the explanation of the operation of the DC/DC converter of FIG. 1 in push-pull configuration, reference is made to the volume mentioned in the introduction with the note that the integrated circuit PWM of the example is UC1846 of UNITRODE but today there are many circuits capable of fulfilling equivalent functions. As mentioned above, these include an oscillator generating a periodic signal with presettable frequency from which are taken two identical pulsed periodic wave forms of period T, and phase-shifted with each other by T/2 which corresponds to the signals Q(t) and Q(t+T/2). The width of the pulses is controlled in negative feedback on the basis of the error signal e with the restraint that it should always be less than T/2. To meet this last requirement, the UC1846 has a pin to act as described in the application notes thereof. The error amplifier OP calculates the difference between the reference voltage present at the ends of the Zener diode Z which is reverse polarized and a fraction of the voltage Vout present at the ends of C2.

The network TRFC makes available the above mentioned fraction of Vout, without breaking the galvanic insulation existing between the primary side circuits and the secondary side circuits and between the respective grounds. This is made possible by the particular circuit configuration of TRFC together with the forms of the signals which control the MOSFETs of IC1 and IC2 and with the choice of suitable points for the application of control signals.

As regards the first point above it is noted that the MOSFETs 1, 2 and 3, 4 are capable of completely disconnecting the contacts between the two ends of C1 and the load Ro, and the MOSFETs 5, 6 and 7, 8 are capable of completely disconnecting the contacts between the two ends of C1 and those of C2. In practice, IC1 comprises a first pair of synchronous electronic switches of which one consists of the MOSFETs 1 and 2 and another of the MOSFETs 3 and 4. Similarly, IC2 comprises a second pair of synchronous electronic switches, of which one consists of the MOSFETs 5 and 6 and another of the MOSFETs 7 and 8. It is therefore possible circuitally to charge C1 at the voltage Vout regardless of the charge in C2, and in an equivalent manner it is possible to transfer the charge of C1 and C2 regardless of the voltage Vout. As mentioned below, it is just the independence of the above operations which preserves the galvanic insulation. In

the open state the MOSFETs used are capable of withstanding voltages on the order of 400V and, as they are of the enhancement type, they remain open even with null voltage on the source electrode. In the conduction state the MOSFETs exhibit an entirely negligible channel resistance, noting that of the two MOSFETs connected in series which provide a generic electronic switch, one is always forward polarized and the other reversed. In this manner the diodes formed between the drain-substrate junctions are back-to-back connected, thus eliminating all possible conduction through the substrates and failure of the galvanic insulation. A mistaken choice of the type of transistor, especially when the electronic switches are provided by a single transistor, could cause setting up of a permanent conduction path through the independent substrates from the open or closed state of the electronic switches.

As regards the points where the control signals of IC1 and IC2 come from, it can be seen that these points are insulated galvanically from each other because one belongs to the primary winding P3 and the other to the secondary winding S2 of the transformer TRS. The galvanic insulation between the control signals is held within the TRFC network, since the control signal taken at the secondary winding S2 controls only the IC1 which is always insulated from the primary side circuits as explained below. Similarly the control signal taken at the primary winding P3 controls only IC2 which is always insulated from the secondary side circuits.

A valid and more general alternative consists of connecting the control input of IC2 to an output of the integrated circuit PWM while keeping unchanged the connection between the control input of IC1 and the end of the secondary winding S2 which supplies the suitable signal.

The form of the control signals of IC1 and IC2 is that produced at the ends of the primary and secondary windings of the transformer TRS due to the switching effect of TR1 and TR2. The voltages at the ends of P1, P2, P3, S1 and S2 are pulses of the same width as those belonging to Q(t) and Q(t+T/2) but with polarities inverting every half-period T/2. For the purposes of their use for control of TRFC, it is necessary to pick-up the voltage at the primary winding P3 and the secondary winding S2 with opposite polarities, and then to rectify them half-wave, by using the positive half-waves for control of IC2 and IC1 respectively. In practice, the rectification is made by the MOSFETs and it is thus sufficient to connect P3 and S2 to the respective control point of IC2 and IC1.

It remains to be seen if a breakdown of the insulation could occur during transfer of the voltage Vout between the input and the output of TRFC controlled by the above mentioned signals. These control signals sub-divide the operation of the charge-transfer network TRFC in four sequential phases which are repeated

every period T without regard for starting order. Let us assume for example that the control signal corresponding to Q(t) is applied to IC1 and that corresponding to Q(t+T/2) is applied to IC2 starting from an initial state wherein the converter is off and the above mentioned signals are constrained to their respective ground potentials. In the initial state the two switch pairs IC1 and iC2 are both open and it follows that C1 and C2 are discharged and C1 is insulated both from Ro and C2.

During a first of the four operating phases an active control pulse reaches IC1 producing closing of the respective switch pair, and connecting one end of C1 to the output terminal of the converter and the other end to the secondary ground. C1 is charged at the value Vout through the resistance R1. At the same time the control signal on IC2 is null and the switch pair IC2 is open and insulates C1 from the circuits connected to the primary of TRS. The charge time constant R1C1 is small enough to allow complete charging of C1, even if the control pulse has minimal duration.

In a second phase the two control signals are both null, and in this case C1 is loaded and insulated both from Ro and from C2. This second phase is ever present because the duration of the control pulses is still less than T/2.

In a third phase an active control pulse reaches IC2 producing closing of the respective switch pair and connecting C1 in parallel with C2 and allowing charge-transfer between C1 and C2. In the meantime the control signal on IC1 is null and the switch pair IC1 is open and insulates C1 and C2 from the secondary side circuits of TRS. The charge-transfer takes place almost instantaneously and the duration is limited only by the very low channel resistance of the MOSFETs 5, 6, 7 and 8. The parallel between the two capacitors remains for the entire duration of the active pulse, and during this time the charge accumulated in the two capacitors is discharged through R2 with a time constant given by the product of R2 times C1+C2.

In a fourth and last phase the two control signals are again both null and in this case the parallel between C1 and C2 is disconnected, and again in this case the same remarks made for the second phase apply.

In view of the foregoing discussion, synchronous operation of the two switch pairs IC1 and IC2 is absolutely excluded and the formation of a connection path between them with the possibility of breaking the galvanic insulation even briefly during the open/close transients is prevented.

At this point it is useful to make some additional remarks on the values of R1, C1, R2 and C2. A first requirement is that the time constants R1C1 and R2C2 be small so that the respective poles introduced in the frequency response of the system will fall far above the upper end of the loop band, which in the example is

approximately 12 kHz. In this manner their existence does not disturb the stability of the converter. In practice, considering the Bode diagram of the loop gain, it is sufficient that these poles be at least one decade higher than the band end. A second requirement is that the voltage Vout on C1 be not reduced too much on the parallel of C1 with C2, and this limits the value of C2. This value should however always be greater than that of C1 to cause the charge to be accumulated predominantly on C2 after completion of the transfer. In this manner C2 can act as a "memory" when the connection with C1 is broken before completion of the discharge, and this occurs when the duration of the control pulses of IC2 is minimal. A good choice is e.g. C2 = 4C1. The value of R2 should be such as to not allow a too fast discharge of the capacitor equivalent of the parallel C1 and C2, or of only C2 compatibly with the period T, because otherwise there would derive therefrom an error signal consisting of narrow pulses. In this case the energy would fall predominantly on the components placed outside the loop band.

The remarks made for the DC/DC converter of the example are also applicable for circuit configurations other than push-pull, provided they include a transformer to insulate the load from the primary power supply source. Configurations comprising a single power transistor have primary and secondary voltages in which the pulse in the half period fails. The fact causes no particular problem concerning control of the TRFC network since it is only necessary to connect the control input of IC2 directly to the control output of PWM which does not pilot the power transistor, while for control of IC1 the signal is taken at the secondary as in the example.

Devices different from those indicated can be used as electronic switches and the remarks made are in all cases sufficient for one of ordinary skill in the art to seek the wave form each time most suitable for control of the charge-transfer network using the selected devices.

CLAIMS

1. DC/DC converter comprising one or more power devices (TR1,TR2) acting as electronic switches which cyclically open and close the connection between a battery and the primary of a transformer (TRS), whose secondary voltage supplies a rectifier circuit connected to the output terminal of the converter, to which is connected a load (Ro), and to a secondary ground insulated galvanically from the primary battery ground; said converter comprises also control circuits (PWM) supplied on the primary side and essentially consisting of: (a) an oscillator driving a logic circuit for obtaining two identical periodic wave forms of period T, and phase-shifted with each other by T/2, and consisting of pulses (Q(t),Q(t+T/2)) used or usable for control of the conduction state of the power devices, (b) a generator of a constant temperature-stable reference voltage, c) a circuit (OP) finding the difference between said reference voltage and a fraction of the voltage (Vout) on the load, and obtaining an error signal supplied to a negative feedback regulating circuit (d) of the duration of said control pulses , characterised in that said fraction of the voltage (Vout) on the load is obtained by means of a charge-transfer network (TRFC) comprising:

a first pair of synchronous electronic switches (IC1), controlled by a first control signal, and which connect or disconnect respective ends of a first capacitor (C1) with the output terminal of said power supply or said secondary ground, and allowing the charge of said first capacitor up to a voltage (Vout) at the ends of said load (Ro).

a second pair of synchronous electronic switches (IC2), controlled by a second control signal, and which connect or disconnect said first capacitor (C1) in parallel with a second capacitor (C2) having one end connected to said primary ground, and allowing a charge-transfer between said capacitors (C1,C2) and a resulting generation at the ends of said second capacitor (C2) of said fraction of the load voltage (Ro) used for determining said error (e),

and further characterised in that said first control signal corresponds to a first said pulsed periodic wave form Q(t), Q(t+T/2) transferred to the secondary (S2) of said transformer (TRS), and said first pair of synchronous electronic switches (IC1) being closed at said control pulses,

and in that said second control signal is a said second pulsed periodic wave form (Q(t+T/2),Q(t)) generated on the primary side and said second pair of electronic switches (IC2) being closed at said control pulses,

and in that said control circuit limits to values below T/2 the duration of said control pulses, thus allowing opening of both of said pairs of electronic switches (IC1,IC2) before and after the charging of said first capacitor (C1).

2. DC/DC converter in accordance with claim 1, characterised in that said first pair of electronic switches (IC1) connects said first capacitor (C1) to the ends of said load (Ro) through a first resistance (R1) placed in series with said first capacitor (C1).

3. DC/DC converter in accordance with claim 1, characterised in that said second capacitor (C2) is connected in parallel with a second resistance (R2).

4. DC/DC converter in accordance with claim 2, characterised in that the inverse of the time constant given by the product of 2π times the capacitance of said first capacitor (C1) and times the value of said first resistance (R1), corresponds to a pole of the frequency response of the loop gain of said DC/DC converter, whose value is at least one decade higher than the upper end of said response band.

5. DC/DC converter in accordance with claim 3, characterised in that the inverse of the time constant given by the product of 2π times the capacitance of said second capacitor (C2) and times the value of said second resistance (R2) corresponds to a pole of the frequency response of the loop gain of said DC/DC converter, whose value is at least one decade higher than the upper end of said response band.

6. DC/DC converter in accordance with claim 1, characterised in that the capacitance of said second capacitor (C1) is higher than the capacitance of said first capacitor (C1).

7. DC/DC converter in accordance with claim 1, characterised in that the electronic switches belonging to said pairs of electronic switches (IC1,IC2) are provided by means of MOSFET enhancement transistors 1...4, 5...8), the transistors of each pair having their control electrodes connected together.

8. DC/DC converter in accordance with claim 7, characterised in that said transistors have their substrate connected to the respective source and in that each said electronic switch is provided by means of two of said transistors connected in series with a first transistor forward polarized and a second transistor reverse polarized.

9. DC/DC converter in accordance with claim 1, characterised in that the transfer to the secondary (S2) of said first pulsed periodic wave form (Q(t),Q(t+T/2)) takes place by the effect of the switching of one of said power devices (TR1,TR2) controlled by said first wave form.

10. DC/DC converter in accordance with claim 1, characterised in that the transfer to the secondary (S2) of said first pulsed periodic wave form (Q(t),Q(t+T/2)) takes place by the effect of the switching of said power devices (TR1,TR2) with said first control signal obtained by rectifying with a single half-wave the secondary voltage.

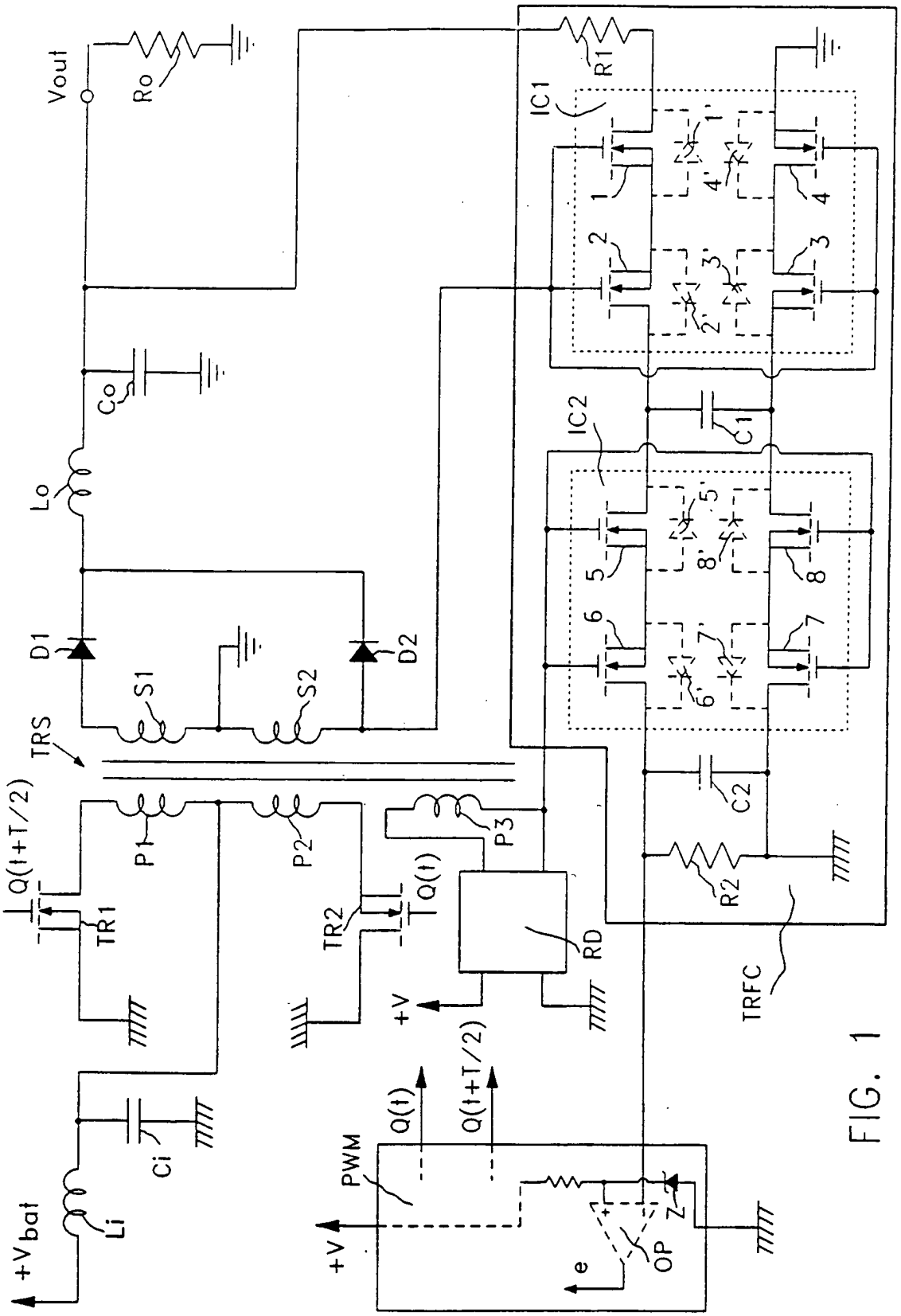
Vout
Ro
Co
Lo
D1
D2
S1
S2
TRS
Q(t+T/2)
TR1
P1
P2
P3
TR2
Q(t)
RD
+V
IC1
IC2
R1
C1
C2
R2
TRFC
+Vbat
Li
Ci
PWM
OP
e
Z

FIG. 1

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 95/01698

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H02M3/337 H02M3/335

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 547 916 (TEXAS INSTRUMENTS INC ;TEXAS INSTRUMENTS LTD (GB)) 23 June 1993 see the whole document ---	1
A	EP,A,0 484 610 (BULL HN INFORMATION SYST) 13 May 1992 see abstract; figure 5 ---	1
A	WO,A,87 03150 (MOTOROLA INC) 21 May 1987 see abstract; figure 1 -----	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
4 August 1995	25. 08. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Gentili, L

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 95/01698

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0547916	23-06-93	NONE	
EP-A-0484610	13-05-92	NONE	
WO-A-8703150	21-05-87	CA-A- 1283166	16-04-91
		JP-T- 63501400	26-05-88
		US-A- 4688158	18-08-87